

IN THE CLAIMS:

Please amend claims 1-4 as shown in the complete list of claims that is presented below.

1. (currently amended) A layout of a flash memory having <sup>a plurality of</sup> symmetric select transistors, comprising:  
a memory cell array;  
<sup>plurality of</sup> a polysilicon gates <sup>of the select transistors</sup> extending in a direction perpendicular to <sup>a side of</sup> the memory cell array and cooperating with a plurality of pairs of <sup>the</sup> sources/drains ~~arranged at two sides thereof~~ for forming <sup>a</sup> ~~a~~ plurality <sup>symmetric</sup> of select transistors; and  
a wires connecting the plurality of select transistors and the memory cell array.

2. (currently amended) The layout according to claim 1, wherein the wires comprises a segments parallel to the polysilicon gates.

3. (currently amended) A layout of a flash memory having <sup>a plurality of</sup> symmetric select transistors, comprising:  
a memory cell array; and <sup>plurality of</sup> a polysilicon gates <sup>of the select transistors</sup> corresponding to <sup>the</sup> a plurality of <sup>symmetric</sup> select transistors <sup>a side of</sup> extending in a direction perpendicular to <sup>a</sup> the memory cell array;  
wherein the plurality of select transistors are arranged substantially symmetric with respect to the memory cell array.

4. (currently amended) The layout according to claim 3, further comprising a metal wires <sup>symmetric</sup> extending from the memory cell array toward the polysilicon gates for connecting the plurality of select transistors to ~~a bit line~~ of the memory cell array.

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Please amend claims 1-4 as shown in the complete list of claims that is presented below.

1. (currently amended) A layout of a flash memory having <sup>a plurality of</sup> symmetric select transistors, comprising:
- a memory cell array;
  - a polysilicon gates <sup>of the plurality of symmetric transistors</sup> extending in a direction perpendicular to <sup>a side of</sup> the memory cell array and cooperating with a plurality of pairs of <sup>+ the</sup> sources/drains ~~arranged at two sides thereof~~ for forming <sup>a</sup> plurality of <sup>symmetric</sup> select transistors; and
  - a wires connecting the plurality of select transistors and the memory cell array.
2. (currently amended) The layout according to claim 1, wherein the wires comprises a segments parallel to the polysilicon gates.
3. (currently amended) A layout of a flash memory having <sup>a plurality of</sup> symmetric select transistors, comprising:
- a memory cell array; and
  - a polysilicon gates <sup>the</sup> corresponding to <sup>symmetric</sup> a plurality of select transistors extending in a direction perpendicular to <sup>a side of</sup> the memory cell array; wherein the plurality of <sup>symmetric</sup> select transistors are arranged substantially <sup>the side of</sup> symmetric with respect to the memory cell array.
4. (currently amended) The layout according to claim 3, further comprising a metal wires extending from the memory cell array toward the polysilicon gates <sup>symmetric</sup> for connecting the plurality of select transistors to ~~a bit line~~ of the memory cell array.